

# ● PRINTER RUSH ●

## (PTO ASSISTANCE)

Application : <u>09692344</u>	Examiner : <u>Bates</u>	GAU : <u>2155</u>
From: <u>ewc</u>	Location: <u>IDC</u> FMF FDC	Date: <u>7-7-05</u>

ATTN: Chief Draftsperson      Tracking #: 06072013      Week Date: 1-31-05

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> Foreign Priority
<input type="checkbox"/> CLM	_____	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW	_____	<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW	_____	<input type="checkbox"/> Other
<input checked="" type="checkbox"/> DRW	<u>1-16-01</u>	
<input type="checkbox"/> OATH	_____	
<input type="checkbox"/> 312	_____	
<input type="checkbox"/> SPEC	_____	

[RUSH] MESSAGE: \_\_\_\_\_

There are horizontal lines through Figures

Thank you

[XRUSH] RESPONSE: \_\_\_\_\_

Drawings corrected

INITIALS: WJ

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.  
REV 10/04

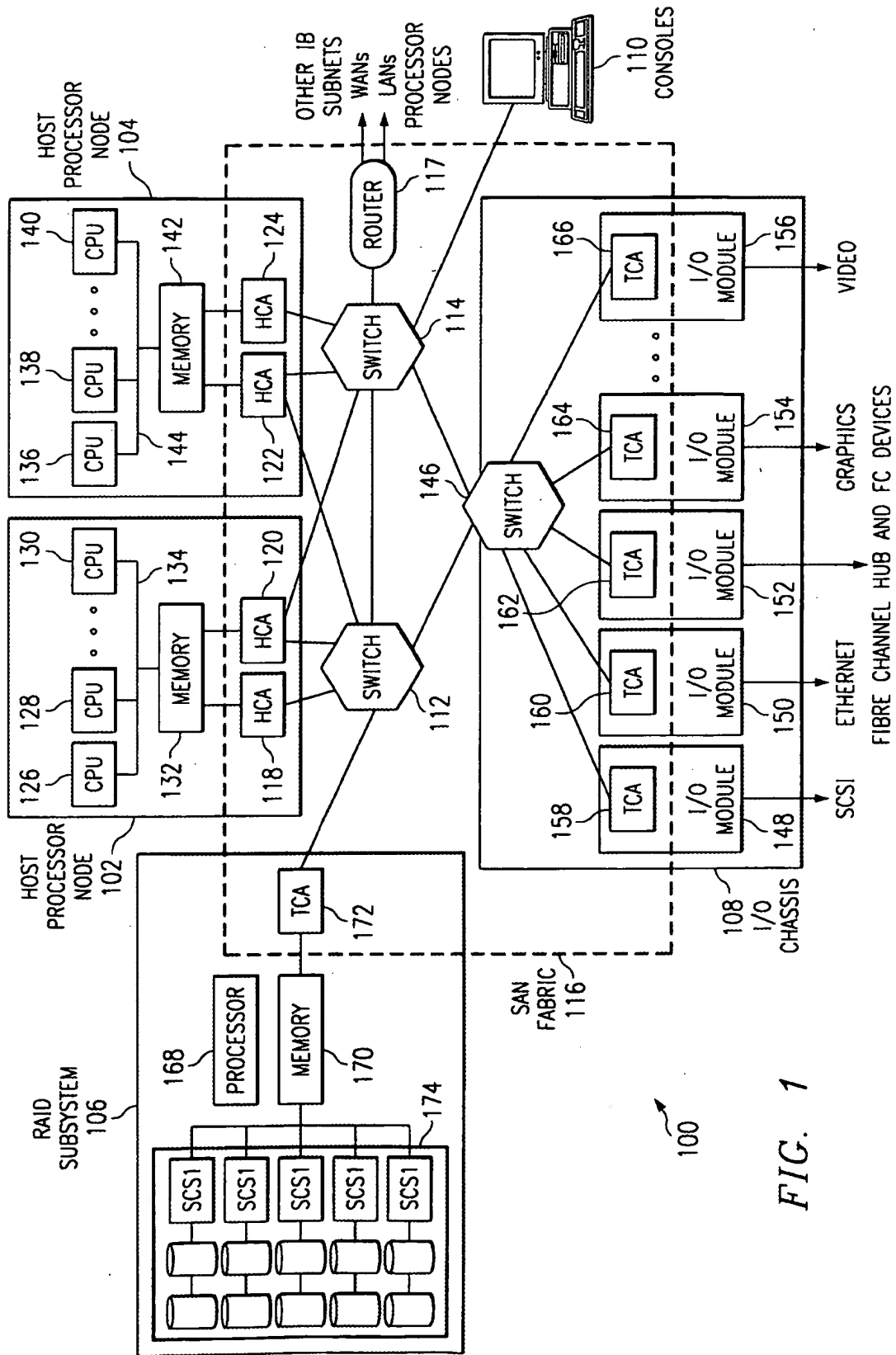


FIG. 1

Diagram illustrating a Host Processor Node (200) architecture. The node includes a MESSAGE AND DATA SERVICE (224) and multiple CONSUMER units (202, 204, 206, 208). These consumers are connected to CHANNEL ADAPTER (ENDNODE) blocks (214, 216, 218, 220) via PORT components (210, 212). A dashed line labeled VERBS separates the service layer from the adapter layer.

G. 3

302 304 MEMORY 310 340 300

QP QP QP QP ... QP

306 DMA 308

CHANNEL ADAPTER

SMA 336

TRANSPORT

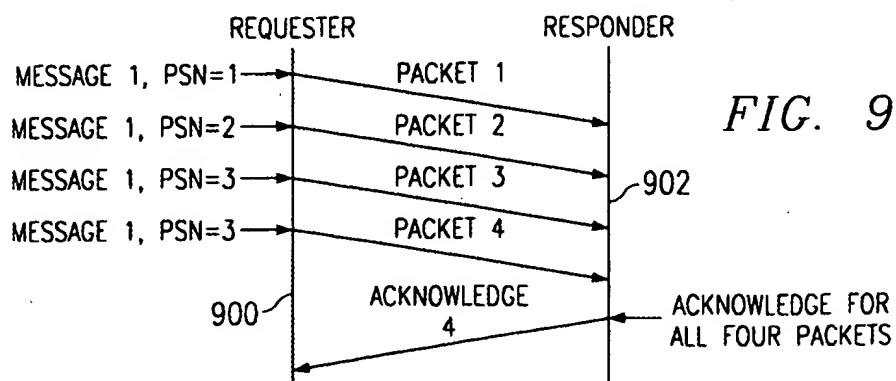
338 MTP

318 320 322 324 326 328 330 332 334

VL VL ... VL VL VL ... VL VL VL ... VL

PORT PORT ... PORT

312 314 316



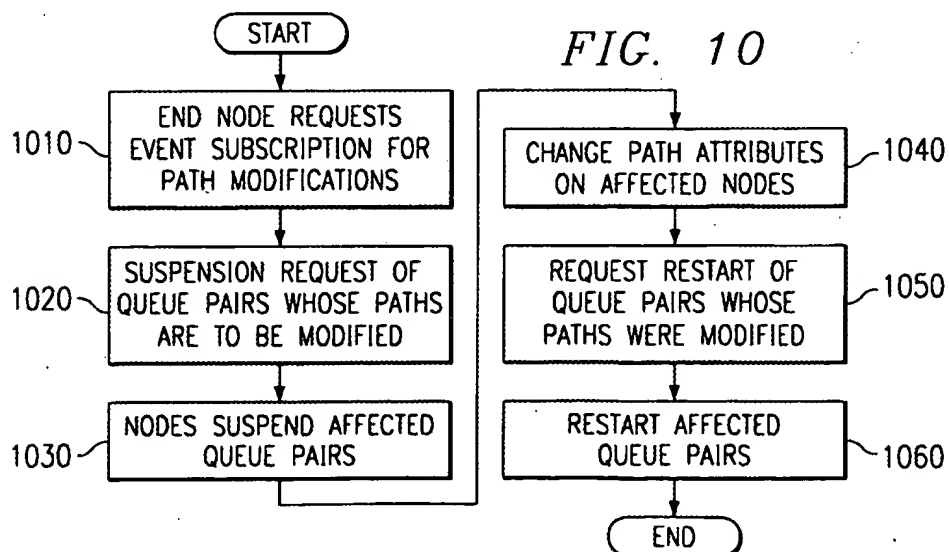
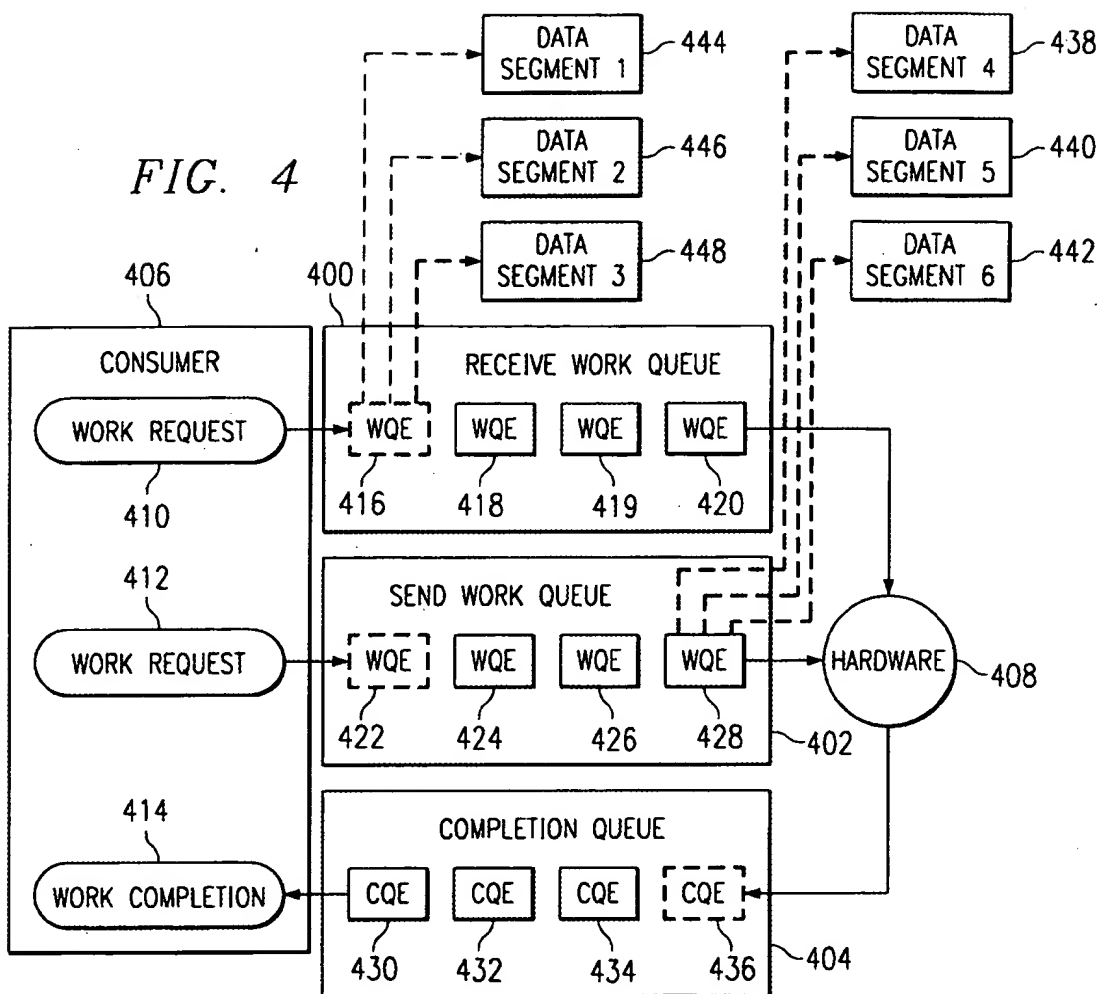


FIG. 5

500

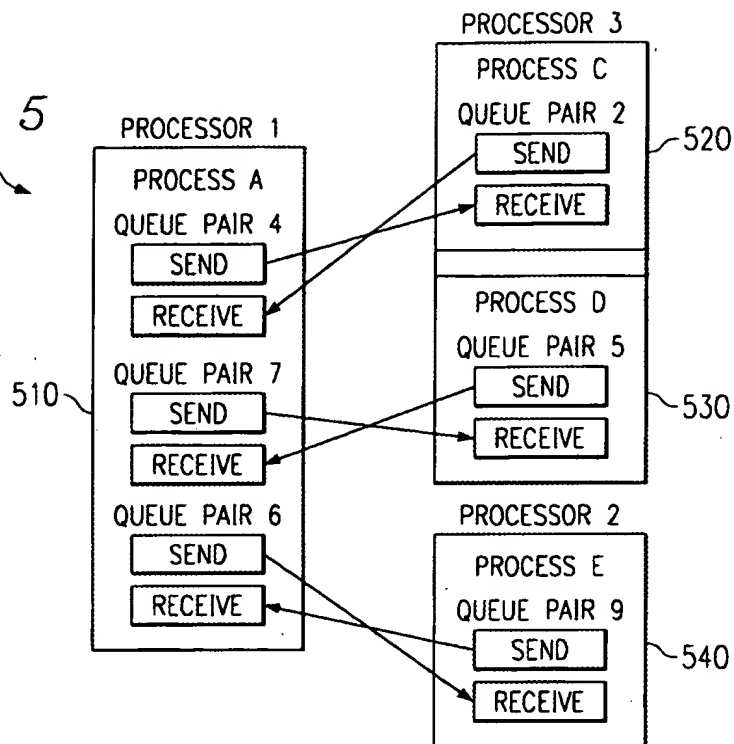


FIG. 6

600

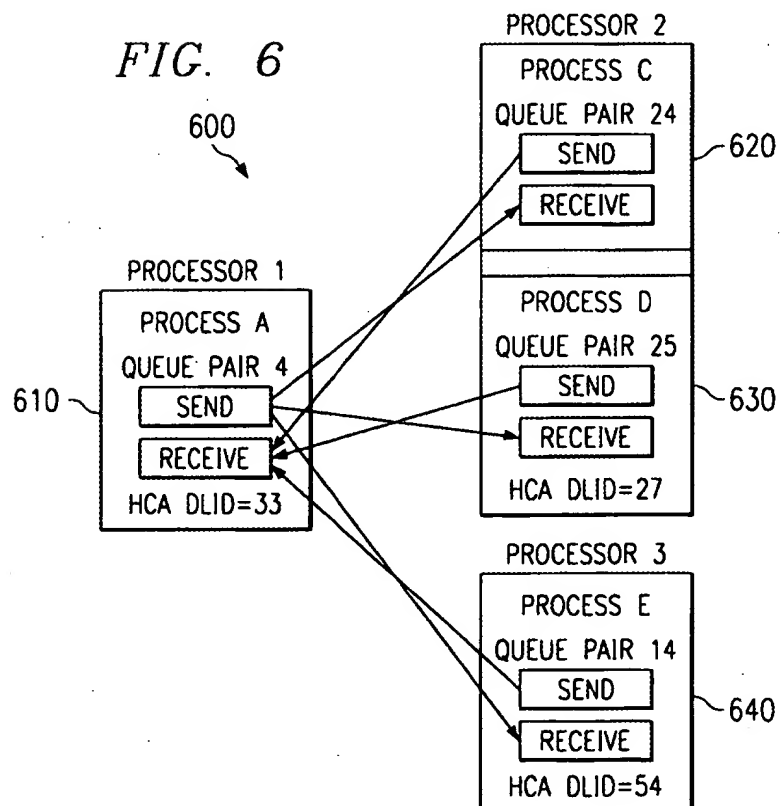


FIG. 7

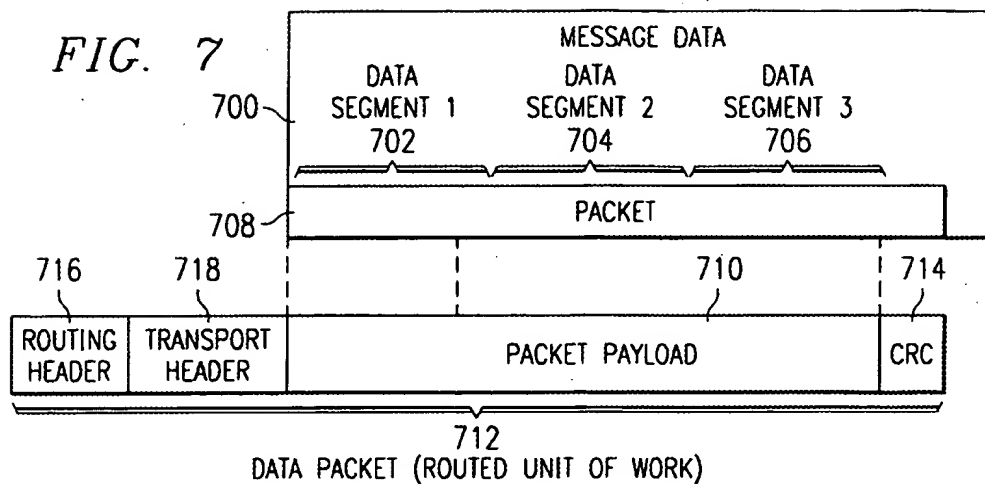


FIG. 8

